Circuit for Compensation Against Back-gating

ABSTRACT OF THE DISCLOSURE

According to the invention, back-gating in a power FET caused by drain voltage changing rapidly from a higher voltage level to a lower voltage level is mitigated by use of a sensing FET that measures current flow whose level corresponds to the degree of back-gating. A compensation signal is generated using a voltage associated with the measure of current flow. A gate voltage is connected with a gate of the sensing FET and a gate of the power FET, wherein the gate voltage is adjusted or generated via a feedback path using the compensation signal such that the adjusted or generated gate voltage compensates against effects of back-gating. The sensing FET is located on a common substrate as the power FET.